In the Claims

The following claims are amended as follows:

1. (Currently amended) A method of determining a fail string for a device comprising the steps of:

determining a portion of an address space to test for determining an occurrence of a fail type, wherein the portion of the address ~~spaces~~ space comprises at least one x ~~addresses~~ address and at least one y ~~addresses~~ address of the device;

executing a test pattern that includes at least one address in the address space at least two times for ~~each~~ the at least one address, wherein ~~each~~ the at least one address is held at a first potential for at least a first test and a second potential for at least a second test;

determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types; and

determining the occurrence of the fail type according to the pass/fail results of a subset of the fail string.

2. (Cancelled)

3. (Original) The method of claim 1, wherein the test pattern includes a single address.

4. (Currently amended) The method of claim 1, further comprising the steps of:

holding each address individually at the first potential during ~~a~~ the first test, yielding in a pass/fail result; and

holding each address individually at the second potential during ~~a~~ the second

test, yielding in a pass/fail result.

5. (Currently amended) The method of claim 1, ~~further comprising the step of executing the test for the test pattern,~~ wherein the test pattern is a combination of at least two addresses.

6. (Currently amended) The method of claim 1, wherein the step of determining the ~~test pattern~~ portion of the address space further includes the step of determining at least one x address and at least one y address according to the fail type to be determined, wherein the fail type to be determined is identified using a subset of the addresses in the address space.

7. (Previously presented) The method of claim 1, further comprising the step of generating a pseudo compressed bitmap comprising a plurality of cells of the x addresses and y addresses needed to determine the fail type, wherein each cell is one of a passing cell and a failing cell.

8. (Previously presented) The method of claim 7, further comprising:

determining the failing cell upon determining a fail in the pass/fail results for every x-y address combination addressing the failing cell; and

determining the passing cell upon determining any one passing x-y address combination addressing the passing cell.

9. (Original) The method of claim 1, further comprising the step of generating a pareto.

10. (Currently amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating a pseudo compressed bitmap for a device, the method steps comprising:

determining a portion of an address space to test for determining an occurrence of a fail type, wherein the portion of the address ~~spaces~~ space comprises at least one x ~~addresses~~ address and at least one y ~~addresses~~ address of the device;

executing a test pattern that includes at least one address in the address space at least two times for ~~each~~ the at least one address, wherein ~~each~~ the at least one address is held at a first potential for at least a first test and a second potential for at least a second test;

determining a fail string for the device including pass/fail results for the test pattern, wherein different subsets of the fail string correspond to different fail types;

generating a pseudo compressed bitmap by combining one or more subsets of the fail string; and

diagnosing a failure of the device according to the pseudo compressed bitmap.

11. (Cancelled).

12. (Original) The method of claim 10, wherein the test pattern includes a single address.

13. (Currently amended) The method of claim 10, further comprising the steps of:

holding each address individually at the first potential during ~~a~~ the first test, yielding in a pass/fail result; and

holding each address individually at the second potential during ~~a~~ the second test, yielding in a pass/fail result.

14. (Currently amended) The method of claim 10, ~~further comprising the step of executing the test for the test pattern,~~ wherein the test pattern is a combination of at least two addresses.

15. (Currently amended) The method of claim 10, wherein the step of determining the ~~test pattern~~ portion of an address space further includes the step of determining at least one x address and at least one y address according to the fail type to be determined, wherein the fail type to be determined is identified using a subset of the addresses in the address space.

16. (Previously presented) The method of claim 10, wherein the pseudo compressed bitmap comprises a plurality of cells of the x addresses and y addresses needed to determine the fail type, wherein each cell is one of a passing cell and a failing cell.

18. (Previously presented) A method of generating a pseudo compressed bitmap for a device comprising the steps of:

generating a pseudo compressed bitmap by combining a plurality of pass/fail results of a fail string; and

displaying the pseudo compressed bitmap wherein the pass/fail results correspond to at least one X address pin and one Y address pin, and wherein each address pin corresponds to a plurality of pass/fail results, wherein a bit is determined to pass in the pseudo compressed bitmap upon determining that any address pin that addresses the bit passes.

19. (Original) The method of claim 18, wherein every combination of a test pattern including at least one address is tested, wherein the combinations include each address held at a first potential for at least a first test and a second potential for at least a second test.